PALM INTRANET

Inventor Information for 10/817572

Inventor Name	City	State/Country
LISSEL, ROBERT	REUTLINGEN	GERMANY
SCHONFELDER, BERND	WEINBOHLA	GERMANY
BARTH, FRANK	RADEBEUL	GERMANY

[Appln Info] [Contents] [Petition Info] [Atty/Agent Info] [Continuity/Reexam] [Foreign [

Search Another: Application# [Search] **or Patent#** [Search]

PCT /   / [Search] **or PG PUBS #** [Search]

Attorney Docket # [Search]

Bar Code # [Search]

To go back use Back button on your browser toolbar.

Back to PALM | ASSIGNMENT | OASIS | Home page

- Drafts
- Pending
- Active
  - L1: (28450) PIO
  - L2: (47288) DMA
  - L3: (593) 1 WITH 2
  - L4: (105) BUFFER WITH 3
  - L5: (4) (('0487812') or ('6708232') or ('6629230') or ('5610808')).l
  - L6: (4) (('4847812') or ('6708232') or ('6629230') or ('5610808')).l
  - L7: (147) (('(6781826') or ('6807600') or ('6811427') or ('6832929')
  - L8: (24) 3 and 7
  - L9: (7) 4 and 7
- Failed
- Saved
- Favorites
- Tagged (10)
- UDC
- Queue
- Trash

Search Lst Browse Create Clear

DBs US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB

Default operator: OR

4 and 7

☑ Plurals
☐ Highlight all hit terms initially

BRS form | S&R form | Image | Text | HTML

	U	1	Document ID ▲	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Cla	Inventor	S	C	P	2	3	
1	☐	☐	US 5592682 A	19970107	47	Interface circuit for transferring data between host device and	710/3			Chejlava, Jr.; Edward J. et al.	☑	☐	☐	☐	☐	☐
2	☐	☐	US 5603052 A	19970211	47	Interface circuit for transferring data between host and mass	710/4	710/307		Chejlava, Jr.; Edward J. et al.	☑	☐	☐	☐	☐	☐
3	☐	☐	US 5630171 A	19970513	47	Translating from a PIO protocol to DMA protocol with a	710/23	710/11; 710/14;		Chejlava, Jr.; Edward J. et al.	☑	☐	☐	☐	☐	☐
4	☐	☐	US 5655145 A	19970805	47	Peripheral interface circuit which snoops commands to	710/1	710/11; 710/22		Chejlava, Jr.; Edward J. et al.	☑	☐	☐	☐	☐	☐
5	☐	☐	US 5826107 A	19981020	46	Method and apparatus for implementing a DMA timeout	710/27	703/24; 710/20;		Cline; Leslie E. et al.	☑	☐	☐	☐	☐	☐
6	☑	☐	US 6567953 B1	20030520	17	Method and apparatus for host-based validating of data	714/805	714/763		Pomerantz; Gregory M.	☐	☐	☐	☐	☐	☐
7	☐	☐	US 6715004 B1	20040330	15	Method and apparatus for intermediate validation of data	710/35	710/22; 710/33;		Grimsrud; Knut S. et al.	☑	☐	☐	☐	☐	☐

Hits | Details | HTML

Ready   NUM

710/22
52,
308
810

710/ 5-7, 20,-28, 33-35
52-57, 308-310

File View Edit Tools Window Help

- Drafts
- Pending
- Active
- Failed
  - S6
- Saved
  - S7: (27) S2 WITH S6
  - S3: (2) LIMIT WITH S2
  - S2: (339) BUFFER NEAR9 INGRESS NEAR9 EGRESS
  - S6: (9241970) COS (CLASS NEAR2 SERVICE)
  - S8: (144) (("6046982") or ("5557607") or ("5570348") or ("5583861")
  - S1: (1) ("20060075188").PN.
  - S5: (1) ("6363385").PN.
  - S4: (1) ("6101497").PN.
  - S10: (3081) buffer and S9
  - S11: (15105) (maximium exceed limit) near9 buffer
  - S9: (4188) (710/5$1).CCLS.
  - S12: (348) S10 and S11
- Favorites
- Tagged (4)
- UDC
- Queue
- Trash

DBs US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB

Default operator: OR

☑ Plurals

☐ Highlight all hit terms initially

BRS form | S&R form | Image | Text | HTML

	U		Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Cla	Inventor	S	C	P				Im
1	☐	☑	US 70 0 0097 B0	2010 1002		System and method and method for allocating shared memory	710/56	370/360;		group of allocating shared	☑		☐			☐	US
2	☐	☑	US 5907717 A	19990525	11	Cross-connected memory system for allocating pool	710/56	370/360; 370/426;		Ellis; Jackson L.	☑	☐	☐	☐	☐	☐	US
3	☐	☑	US 6219728 B1	20010417	18	Method and apparatus for allocating shared memory	710/52	370/229; 370/236;		Yin; Nanying	☑	☐	☐	☐	☐	☐	US
4	☐	☑	US 20030177293 A1	20030918	12	Dynamic memory allocation between inbound and	710/56			Bilak, Mark R. et al.	☑	☐	☐	☐	☐	☐	US

Hits | Details | HTML

Ready

NUM